ABSTRACT

The present invention provides a multichip arrangement and method of arranging multiple chips including at least a first chip (10) and second chip (30). The first chip (10) having opposing top and bottom surfaces in which bonding pads are located on a perimeter of the top surface. The bonding pads are operable for bonding bond wires for coupling the multichip arrangement to a circuit board (40), for example. The second chip (30) also has opposing top and bottom surfaces with bonding pads located on a perimeter of the top surface. In one embodiment an attach layer (220) having an area equal to an area of the second chip bottom surface is applied to the second chip bottom surface. The second chip (30) is coupled to the first chip (10) via the attach layer (220). The attach layer (220) has a thickness to provide electrical disconnection of the first chip wire bonds and the second chip (30). The attach layer (220) is a thermosetting material which is pliable when heated for coupling the first (10) and second chip (30) such that the thermosetting material conforms to the first chip wire bond when the second chip (30) is coupled to the first chip (10). In another embodiment, an insulation layer (230) is applied to the second chip bottom surface prior to application of the attach layer (220) in which the attach (220) layer and the insulation layer (230) are cooperable to provide electrical disconnection of the first chip wire bonds and the second chip.